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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,754	09/03/2003	Stephan G. Meier	6363-00600	3663

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EXAMINER

DILLON, SAMUEL A

ART UNIT	PAPER NUMBER
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2185

NOTIFICATION DATE	DELIVERY MODE
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ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/653,754

Applicant(s)

MEIER ET AL.

Examiner

SAMUEL DILLON

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 November 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,9-13,15 and 21-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,9-13,15 and 21-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Applicant's submission filed on November 4, 2010 has been entered. Per the amendment, Claims 4-8 and 16-20 have been cancelled and Claims 1, 13 and 23 have been amended.

I. RESPONSE TO AMENDMENT(S) / ARGUMENT(S)

2. **Applicant's arguments with respect to the 35 U.S.C. 102(b) and 103(a) rejections of Claims 1, 3, 9-13, 15 and 21-29 have been fully considered and are persuasive, but are moot in view of the new ground(s) of rejection, as described below.**

3. Regarding all other Claims not specifically traversed above and whose rejections were upheld, the Applicant contends that the listed claims are allowable by virtue of their dependence on other allowable claims. As this dependence is the sole rationale put forth for the allowability of said dependent claims, the Applicant is directed to the Examiner's remarks above.

Additionally, any other arguments the Applicant made that were not specifically addressed in this Office Action appeared to directly rely on an argument presented elsewhere in the Applicant's response that was traversed, rendered moot or found persuasive above.

II. REJECTIONS BASED ON PRIOR ART**Claim Rejections - 35 USC ' 103 – Wang and Eberhard**

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claims 25-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US Patent 5,956,746) in view of Eberhard et al. (US Patent 5,713,001).

6. As per **Claims 1 and 13**, but more specifically to Claim 1, Wang discloses a way predictor comprising:

a decoder (*address register, fig 4*) that decodes an indication (*set, bits 5-15, fig 4*) of a first address (*address in the address register, fig 4*) that is to access a cache (*off-processor cache memory, col 2 lns 5-19*) for a current cache access during use, the decoder selecting a set responsive to the indication of the first address during use (*such as set 84, fig 4*);

a memory (*predictor tag array, fig 4*) coupled to the decoder, wherein the memory outputs a plurality of values (*W0 through W3, fig 4*) from a set of storage locations in response to the decoder selecting the set during use, wherein each of the plurality of values corresponds to a different way of a plurality of ways of the memory (*W0 through W3, fig 4*), wherein the cache includes a same number of ways as the memory (*4 ways because cache is 4-way set associative, col 3 lns 53-57*), and wherein the cache includes a tag memory storing a plurality of tags corresponding to cache lines stored in the cache (*remaining tag information, col 3 lns 1-15*) and a data memory storing the cache lines during use (*off-processor cache memory, col 2 lns 5-19*), wherein

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each of the plurality of values comprises a plurality of bits (*4-bits, col 3 lns 58-67*), and wherein each value is associated with a different corresponding cache line stored in the cache in a respective way of the plurality of ways (*col 4 lns 34-45*), and wherein the different corresponding cache line is stored in the set selected by the decoder (*col 4 lns 34-45*), and wherein there is a one-to-one correspondence between the different corresponding cache lines and the of the plurality of values (*4 ways per set, fig 4 and col 4 lns 34-45*), and the plurality of bits forming a given value of the plurality of values, as a whole, is the value associated with the different cache line (*col 3 lns 58-67*); and

a circuit (*comparator, fig 4*) coupled to receive the plurality of values and a first value (*bits 16-19 of the address register, fig 4*) corresponding to the first address and the first value comprising the plurality of bits, wherein the circuit compares the first value to the plurality of values during use (*comparator compares, fig 4*), and wherein a match of the first value and a second value stored in a first way of the plurality of ways causes the circuit to predict the first way be a hit in the cache for the first address for the current access during use (*col 4 lns 10-18*), and wherein the circuit outputs a way identifier identifying the first way to the data memory during use (*way prediction signals, fig 4*), the way identifier used by the data memory to select the first way to output data during use (*col 4 lns 17-22*), and wherein the circuit constructs the way identifier based on the comparisons of the first value to the plurality of values during use (*2-bit signal is output, col 4 lns 10-15*).

For the purposes of this rejection, Wang does not disclose a way prediction generator circuit coupled to receive a first virtual address corresponding to a first address, and wherein the way prediction generator logically combines bits of the first virtual address to generate a first value during use, where each bit of the plurality of bits of the first value is formed from a logical

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combination of two or more virtual address bits from a virtual address that corresponds to the cache line.

Eberhard discloses a generator circuit coupled to receive a first virtual address corresponding to a first address (*col 4 lns 43-56*) wherein the generator logically combines bits of the first original address to generate a first value during use (*col 4 lns 43-56*), where each bit of the plurality of bits of the first value is formed from a logical combination of two or more virtual address bits from an virtual address that corresponds to a given cache line (*exclusive-or is performed on the most significant bits and least significant bits of a virtual address to produce a hashed value of the address, col 4 lns 43-56*).

Wang and Eberhard are analogous art in that they deal with caching and address lookups. At the time of the invention, it would have been obvious to modify Wang to operate using virtual addresses and to hash the stored address tags and compared them against a hashed portion of the address, per the teachings of Eberhard. The motivation for using virtual addresses would have been that virtual addressing provides a larger address space, and the motivation for hashing would have been that it could avoid thrashing (*Eberhard, col 4 lns 30-43*). Therefore, it would have been obvious to modify Wang per the teachings of Eberhard for the benefit of thrashing reduction.

7. As per **Claims 3 and 15**, but more specifically to Claim 3, Wang and Eberhard disclose(s) the circuit, responsive to none of the plurality of values matching the first value in the current cache access, asserts an early miss signal during use, wherein the early miss signal indicates that the first address is a miss in the cache for the current cache access prior to a tag comparison between the first address and the plurality of tags for the current cache access (*none of the four numbers matching causes there to be inherently some signal issues that causes the processor to look elsewhere, col 4 lns 8-11*).

8. As per **Claim 9 and 21**, but more specifically to **Claim 9**, **Wang** and **Eberhard** disclose(s) the indication of the first address comprises at least a portion of the first address (*fig 4*).
9. As per **Claim 10**, **Wang** disclose(s) the indication of the first address comprises two or more address operands used to generate the first address (*address register, fig 4*).
10. As per **Claim 11**, **Wang** and **Eberhard** disclose(s) if the way prediction is incorrect, the cache replaces a cache line in the way indicated by the way prediction with a missing cache line corresponding to the first address during use (*col 4 lns 7-11*).
11. As per **Claim 23**, **Wang** and **Eberhard** disclose(s) an apparatus comprising the way predictor of **Claim 1**, and the data cache data memory coupled to the way predictor (*by way of the cache controller, fig 3*), wherein the data cache data memory is arranged into the plurality of ways (*col 4 lns 34-45*), and wherein the data cache data memory outputs data from the first way during use (*col 5 ln 66 to col 6 ln 2*), and wherein the data cache data memory includes a second circuit that reduces power consumption attributable to one or more non-predicted ways of the plurality of ways during use (*if none of the four numbers match, a cache miss is detected without having to compare against the remaining tag bits, col 4 lns 7-11*).
12. As per **Claim 24**, **Wang** and **Eberhard** disclose(s) the data cache tag memory outputting a tag from the first way and not outputting tags from the one or more non-predicted ways during use (*the predicted way has the remaining tag compared against, the non-predicted ways do not, col 5 ln 66 to col 6 ln 2*).
13. As per **Claim 29**, **Wang** and **Eberhard** disclose(s) the apparatus further comprising a second level cache (*the Examiner takes official notice that cache hierarchies are well known in the art, and that it would have been obvious to include a lower level cache for the benefit of additional caching*), and wherein the circuit detects a miss responsive to the plurality of values and the first value prior to the miss being detected in the cache that corresponds to the data

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cache data memory during use (*col 4 lns 7-11*), and wherein the circuit signals the miss to the second level cache during use, and wherein the second level cache begins an access corresponding to the first address responsive to signal from the circuit during use (*per above, cache misses propagate down the hierarchy to a lower level cache*).

Claim Rejections - 35 USC ' 103 – Wang, Eberhard and Tran

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. **Claims 25-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (*US Patent 5,956,746*) and Eberhard et al. (*US Patent 5,713,001*) as combined above with respect to Claim 1, in further view of Tran (*US Patent 6,115,792*).

16. As per **Claim 25**, Wang and Eberhard disclose the apparatus of Claim 23, but for the purposes of this rejection does not disclose the further limitations of Claim 25. Wang discloses the output of a comparison picking which of a plurality of possible 2-bit values are chosen to be output as a way prediction (*col 4 lns 1-22*), but does not disclose how this is done.

Tran discloses generating separate wordlines for each of a plurality of ways in a data cache data memory during use, and wherein a second circuit activates a first wordline to the first way and to not activate word lines to the non-predicted ways during use (*the Row Drive(n)'s pick word lines based on the predicted way from the set of word lines that could be outputted, figure 5*). Wang, Eberhard and Tran are analogous art in that they deal with way prediction. At the time of the invention, it would have been obvious to modify Wang to use Tran's wordline activation system to select the way to output. The motivation for doing so would have been that

it combines prior art elements according to known methods to yield predictable results.

Therefore, it would have been obvious to modify Wang and Eberhard per the teachings of Tran to obtain the invention of Claim 25.

17. As per Claim 26, Wang, Eberhard and Tran discloses the second circuit includes column multiplexor circuitry (*Tran, column select 82 and element 84 and the like, figure 5*) coupled to the plurality of ways, wherein the column multiplexor circuitry selects the output of the first way as input to a sense amplifier circuit, wherein the column multiplexor circuitry is controlled by the predicted first way (*one of the inputs is a result of the predicted first way, so can be said to be controller by said way, figures 4 and 5*).

18. As per Claim 27, Wang, Eberhard and Tran discloses the second circuit includes column multiplexor circuitry (*Tran, column select 82 and element 84 and the like, figure 5*) coupled to the plurality of ways, wherein the column multiplexor circuitry selects the output of the first way as input to a sense amplifier circuit during use, wherein the column multiplexor circuitry is controlled by the predicted first way (*Tran, one of the inputs is a result of the predicted first way, so can be said to be controller by said way, figures 4 and 5*).

19. As per Claim 28, Wang, Eberhard and Tran discloses the second circuit comprises a plurality of sense amplifier circuits (*Tran, col. 14 lines 5-16*), wherein each of the plurality of sense amplifier circuits is coupled to a respective one of the plurality of ways, and wherein each of the plurality of sense amplifier circuits includes an enable input that is controlled by the predicted first way (*Tran, figures 4 and 5*).

Claim Rejections - 35 USC ' 103 – Wang, Eberhard and Wickeraad

20. **Claims 12 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (*US Patent 5,956,746*) and Eberhard et al. (*US Patent 5,713,001*) as combined above with respect to Claim 1, in further view of Wickeraad et al (*US Patent No. 6,490,654*).

21. As per **Claims 12 and 22**, but more specifically to Claim 12, Wang and Eberhard fail to disclose if no way prediction is generated and a cache miss results for the first address, the cache uses a replacement algorithm to select the cache line to be replaced with the missing cache line during use. Wickeraad discloses a cache memory replacement algorithm that replaces cache lines based on the likelihood that cache lines will not be needed soon (*col. 4, lines 50- 52*). Wang, Eberhard and Wickeraad are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Wickeraad suggests that it would have been desirable to incorporate a cache line replacement algorithm into the system of Wang because this allows data which is likely needed soon is assigned a higher replacement class, while data that is more speculative and less likely to be needed soon is assigned a lower replacement class (*col. 5, lines 2-6*). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Wang and Eberhard as suggested by Wickeraad to incorporate the feature as claimed.

22. The Examiner has pointed particular references contained in the prior art of record in the body of this action for the convenience of the Applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply. The Applicant, in preparing the response, should consider fully the entire reference as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

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III. CLOSING COMMENTS

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP ' 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

a. STATUS OF CLAIMS IN THE APPLICATION

24. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(1). CLAIMS NO LONGER IN THE APPLICATION

25. Claims 2, 4-8, 14 and 16-20 were cancelled by amendment.

a(2). CLAIMS REJECTED IN THE APPLICATION

26. Claims 1, 3, 9-13, 15 and 21-29 are subject of a final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 9:30-6:00.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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IMPORTANT NOTE

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185

Sam Dillon
Examiner
Art Unit 2185